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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/531,123	10/13/2005	Stephan Bolz	S3-02P16504	4548

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LERNER GREENBERG STEMER LLP
P O BOX 2480
HOLLYWOOD, FL 33022-2480

EXAMINER	
CAVALLARI, DANIEL J	

ART UNIT	PAPER NUMBER
2836	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/531,123	BOLZ ET AL.	
	Examiner	Art Unit	
	Daniel Cavallari	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5 and 6* is/are rejected.

7)☒ Claim(s) *7 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 April 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/11/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The Examiner acknowledges the amendments submitted 4/11/2005. The cancellation of claims 1-4 and new claims 5-8 are accepted.

Specification

The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.
(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
(d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT.
(e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC.
(f) BACKGROUND OF THE INVENTION.
    (1) Field of the Invention.
    (2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
(g) BRIEF SUMMARY OF THE INVENTION.
(h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
(i) DETAILED DESCRIPTION OF THE INVENTION.
(j) CLAIM OR CLAIMS (commencing on a separate sheet).
(k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
(l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

The Examiner notes the Specification appears to include all the applicable parts however fails to provide the appropriate section headings as shown above (Specifically parts a, f, g, h, & i).

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description:

- References "E" and "Vdiff" described in the Specification)Page 5, Lines 25-33) fail to be provided in the drawings.

The drawings are further objected to because:

- The Specification (Page 6, Lines 5-10) and drawings (Figure 2) fails to identify the resistor which is provided in the drawing but not given a reference number (however is referenced in Figure 3).

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate

changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

Claim 6 is objected to because of the following informalities:

The claim recites the limitation "...a control voltage Vst as a transfer gate to a non-conductive off-state..."

1. Reference characters corresponding to elements recited in the detailed description of the drawings and used in conjunction with the recitation of the same element or group of elements in the claims should be enclosed within parentheses so as to avoid confusion with other numbers or characters which may appear in the claims. See MPEP § 608.01(m).
2. The claim appears to be grammatically incorrect and the phrase is overall confusing making it unclear what is being claimed. Specifically, it is unclear what is meant by a "control voltage as a transfer gate..." The claim will be examined as best understood wherein a control voltage is applied to a transfer gate of the transistor "...a control voltage (Vst) at a transfer gate..."

Appropriate correction is required.

Claim 6 recites "at least one diode assigned to each transistor or group of transistors for recording a chip temperature" and "a temperature recording unit" however the device does not actually "record" the temperature which would involve some form of memory to store the value. Rather, the device "determines" the temperature and has a temperature "comparison" unit for comparing the measured temperature value with a reference temperature value and controls the charge pump accordingly. The Examiner suggests "record" be replaced with "measure, detect, or determine".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 5 is rejected under 35 U.S.C. 102(b) as being anticipated by Ohshima (JP 2000-299634).

A method for switching a semiconductor power switch, which comprises the following steps:

- Providing a semiconductor power switch (QA2, Figure 7B) with a switching path having a resistance and a control input (The control input being the control

voltage applied to the gate of the transistor) [The Examiner notes the switching path has resistance by the mere fact it is not an ideal conductor and further comprises resistance by the switch itself].

- Controlling the resistance of the switching path of the semiconductor power switch via the control input by at least one of a control voltage and a control current in dependence on a chip temperature to maintain the chip temperature of the power switch at a predetermined setpoint temperature (See Column 26, Lines 1-45), and thereby increasing the resistance of the switching path when the setpoint temperature is reached (read on by opening the switch).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yabe et al. (US 2002/0118502) in view of Kubota (US 5,541,549).

Yabe et al. (hereinafter referred to as Yabe) teaches:

A device comprising:

- Semiconductor power switch (Q, Figure 2) having a switching path, and a control input (gate control input) for controlling said power switch with a control voltage to a transfer gate to a non-conductive off-state or to a conductive on-state.
- In an off-state of said power switch, the transistors is blocked (opened, See Paragraph 0109 & Figure 10, "Switch Input")
- At least one diode assigned to each transistor or group of transistors (See Figure 1B) for measuring a chip temperature.
- A charge pump (B, Figure 7) for generating the control voltage, said charge pump driving said transistors of said power switch, in the conductive on-state, in each case only to such an extent that the chip temperature of each transistor of said power switch is maintained at a predetermined setpoint temperature (See Paragraph 0109 & Figure 10, "Switch Input")
- A temperature recording unit ("DT1", Figure 6 & "GC", Figure 2) configured to compare the chip temperature with the predetermined setpoint temperature (B2, Figure 6 & Paragraph 0072) and to output an enable signal representing a result of the comparison to said charge pump (Ls, Figure 2 & B of LS, Figure 7), and wherein a resistance of said switching path is increased when the setpoint temperature is reached (wherein the switch is opened, See Figure 10).

[The Examiner notes it has been held that a preamble is denied the effect of a limitation where the claim drawn to a structure and the portion of the claim following the preamble is a self-contained description of the structure not depending for

completeness upon the introductory clause. *Kropa v. Robie, 88 USPQ 478 (CCPA 1951)*].

Yabe teaches a plurality of switches (See figure 19) each having there own temperature sensing diodes but fails to teach said power switch having two transistors or groups of transistors connected in series.

Kubuta teaches a power switch (Figure 1A) comprising two transistors in series. It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate two series connected transistors as taught by Kubota in place of a single transistor as taught by Yabe. The motivation would have been to provide redundancy in the switching device for better reliability (eg. in case one switch does not open upon being signaled upon the other switch is still available to open and disconnect the circuit).

The Examiner further notes that it has been held that the mere duplication of essential working parts of a device has no patentable significance unless a new and unexpected result is produced. *In re Harza, 124 USPQ 378.*

Allowable Subject Matter

Claims 7 & 8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 7 recites particulars of the power switch wherein the switch comprises two transistors connected in series with interconnected gate and source terminals which further comprise a transistor connected to said transfer gate with a collector-emitter path between said interconnected gate connections and said interconnected source connections of two transistors, said further transistor being connected to receive an external signal for switching into a conductive state and for rapidly rendering said transfer gate non-conductive.

Although prior art Bolz et al. (US 2006/0034138) teaches such a switch configuration there is a lack of motivation to incorporate said particular switch configuration with the device of Yabe.

Claim 8 recites the particular temperature recording circuitry of Figure 3 which comprises a series circuit, connected to poles of a voltage source, and respectively assigned diode, and a resistor for each transistor, wherein a node between said resistor and said diode, at which a voltage representing the chip temperature is present which further comprises a plurality of comparators each having a first input connected to a respective said node between said resistor and said diode, a second input receiving a nominal voltage representing the setpoint temperature, and an output wherein said comparators performing a comparison between the voltage representing the chip temperature and the nominal voltage representing the setpoint temperature further comprises a first logic element having an input connected to said outputs of said comparators, and an output and a second logic element having a first input connected

to said output of said first logic element, a second input connected to receive an ON/OFF signal, and an output outputting an output signal wherein said output of said second logic element is connected to a gate oscillator of said charge pump as an enable signal. Prior art of record fails to teach this particular temperature recording structure incorporated with the particular semiconductor switch structure.

Conclusion

For examination purposes, Oshima (US 6,392,859) has been taken to be the English equivalent of Oshima (JP2000-299634).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel Cavallari whose telephone number is 571-272-8541. The examiner can normally be reached on Monday-Friday 9:00am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on (571)272-2800 x36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Daniel Cavallari

December 7, 2007

12/10/A

MICHAEL SHECHTY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800